REMARKS

Claims 1-24 are pending in the present application. Claims 1-3, 5, 10-12, and 14 are amended. Claims 19-24 are added. Reconsideration of the claims is respectfully requested.

Also, a Replacement Page is submitted for Figures 1 and 2 with a correction to Figure 2, as suggested by the Examiner. These changes will be incorporated into a formal set of drawings upon approval of the proposed changes by the examiner.

I. 35 U.S.C. § 101

The Office Action rejects claim 1 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. Claim 1 is amended to overcome the rejection.

II. 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 1-9, 12, and 13 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

As to claims 1-9, 12, and 13, the Office Action states:

> Claim 1 recites the limitation "bus design" in line 1. A "design" refers to a concept, and is therefore directed to non-statutory subject matter. The Examiner recommends changing "bus design" in claim 1, line 1 to --bus apparatus--. (It should be noted that for examination purposes, "bus design" has been interpreted as --bus apparatus--).
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> Claim 3 recites the limitation "the resistors" in line 1. There is insufficient antecedent basis for this limitation in the claim.
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> Claim 12 recites the limitation "the resistors" in line 2. There is insufficient antecedent basis for this limitation in the claim.
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> Dependent claims 2-9 and 13 inherit the deficiencies of claims 1 and 12, respectively.

Claims 1, 3, and 12 are amended to overcome the rejection.

III. 35 U.S.C. § 103, Obviousness

The Office Action rejected claims 1-4, 9-13, and 18 under 35 U.S.C. § 103 as being unpatentable over the Admitted Prior Art ("APA") in view of *Poulton et al.* (U.S. Patent No. 6,556,628). This rejection is respectfully traversed.

With respect to claims 1-4, 9-13, and 18, the Office Action states:

> With regard to independent claim 1 and as shown in Fig. 2 of the present application, the APA discloses a bus, including a clock driver (item 210), a clock receiver (item 220) coupled to the clock driver by two clock bus lines (items 270 and 272) carrying complementary clock pulses, a plurality of drivers (items 202, 204, and 206) a plurality of receivers (items 221, 214, and 216) each coupled to a respective one of the plurality of drivers by bus lines (items 262, 264, and 266). With regard to dependent claim 9, the APA teaches the bus, further including a plurality of outputs (items 282, 284, and 286) from the data receivers coupled to a deskew/retiming logic component (item 240).
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> With regard to independent claim 10 and dependent claims 11-13, and 18, and as shown in Fig. 1 of the present application, the APA discloses a data processing system (item 100), including a plurality of components (*e.g.*, items 102, 108, 104, etc.), and a bus (item 106) coupling at least two of the plurality of components. The APA also discloses the features of claims 10 and 18 as described with respect to claims 1 and 9 above.
>
> The APA does not expressly disclose the bus or the data processing system where the receivers detect signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses, as described in independent claims 1 and 10. Poulton discloses receivers (Fig. 4, receivers Y and Y') detecting signals on respective bus lines (Fig. 4, bus lines Y and Y') with respect to a reference voltage derived from a combination of complementary pulses (see column 2, lines 20-45).
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> The APA also fails to expressly disclose the bus or the data processing system, where the reference voltage is derived from a resistive connection between the complementary clock pulses, as described in dependent claims 2 and 11. Poulton teaches (Fig. 4) a reference voltage that is derived from a resistive connection between complementary pulses.
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> The APA also fails to expressly disclose the bus or the data processing system, where resistors in the resistive connection have approximately equivalent resistance, as described in dependent claims 3 and 12. Poulton teaches resistors in the resistive connection that have approximately equivalent resistance (column 6, lines 51-65).
>
> The APA also fails to expressly disclose the bus, where the resistance is approximately equivalent to the resistance of the bus lines, as described in dependent claim 4, and the data processing system, where the resistance is approximately 50 ohms. Poulton teaches a resistance that is

approximately equivalent to the resistance of the bus lines (column 6, lines 54-57) and a resistance that is approximately 50 ohms (column 6, lines 51-65).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the driver, receiver, and resistor configuration of Poulton with the APA. The suggestion or motivation for doing so would have been to alleviate the problems of increased power consumption caused by the use of a conventional single-ended signaling system (column 1, lines 54-55), such as the local V_{ref} disclosed in the APA. Furthermore, the driver, receiver, and resistor configuration disclosed in Poulton alleviates the noise introduced in the signal transmitted over the bus lines, which may result in bit errors in the output from the receiver (column 1, lines 64-67). Even further, the driver, receiver, and resistor configuration of Poulton provides a larger signal swing for detection by the receiver than single-ended systems (column 2, lines 46-57). Finally, the sizing of the resistors in Poulton helps to reduce reflections in the system (column 6, lines 60-65).

Therefore, it would have been obvious to combine Poulton with the APA to obtain the invention as specified in claims 1-4, 9-13, and 18.

Office action, dated October 27, 2003. Claims 1 and 10 are amended to recite a bus apparatus wherein said reference voltage is derived from a resistive connection between said complementary clock pulses and wherein each clock bus line is split terminated such that each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair. Claim 1, as amended, recites:

1. A bus apparatus, comprising:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by data bus lines, said receivers detecting signals on respective data bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses,

wherein said reference voltage is derived from a resistive connection between said complementary clock pulses; and

wherein each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair.

Poulton fails to teach or suggest a reference voltage being derived from a resistive connection between complementary clock pulses, as recited in claim 1. The cited portion of *Poulton* states:

> FIG. 2 illustrates an example of a conventional differential signaling system. In FIG. 2, a transmitter 200 converts an input stream of binary data bits into a pair of equal and opposite currents at its outputs. The currents are transmitted through a pair of conductors 201 and 202 to a receiver 203. In order to transmit a logical "1" to the receiver 203, the transmitter 200 generates current flowing towards the receiver on the conductor 201 and an equal but opposite current flowing towards the transmitter 200 on the conductor 202. Similarly, in order to transmit a logical "0", the transmitter generates a current flowing towards the transmitter on the conductor 201 and an equal but opposite current flowing towards the receiver 203 on the conductor 202.
>
> In order to decode the received signals, the receiver 203 detects the voltage difference between ends 204 and 205 of a resistive terminator 206. If the voltage difference is positive, i.e., the voltage at end 204 is higher than the voltage at end 205, the receiver 203 may output a logical "1". If the voltage difference is negative, i.e., the voltage at the end 204 is lower than the voltage at the end 205, the receiver 203 may output a logical "0". In addition to converting the currents on the conductors 201 and 202 into voltages, the terminator 206 also reduces reflections on the conductors 201 and 202.

Poulton, col. 2, lines 20-45. This cited portion describes an example of a conventional differential signaling system. This portion of *Poulton* does not describe, in any way, deriving a reference voltage from complementary clock pulses. In fact, no portion of *Poulton* teaches or suggests deriving a reference voltage from complementary **clock** pulses.

Furthermore, the allegedly admitted prior art and *Poulton*, taken alone or in combination, fail to teach or suggest "wherein each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair," as recited in amended claim 1. The applied prior art fails to teach or suggest each and every claim limitation; therefore, claim 1 cannot be rendered obvious by the proposed combination of allegedly admitted prior art and *Poulton*.

Independent claim 10 recites subject matter addressed above and is allowable for the same reasons. Since claims 2-4, 9, 11-13, and 18, as well as new claims 19-22 depend from claims 1 and 10, the same distinctions between the allegedly admitted prior

art and *Poulton* and the invention recited in claims 1 and 10 apply for these claims. Additionally, claims 2-4, 9, 11-13, and 18-22 recite other additional combinations of features not suggested by the reference.

Therefore, the rejection of claims 1-4, 9-13, and 18 under 35 U.S.C. § 103 is overcome.

The Office Action rejects claims 1-3, 9-12, and 18 under 35 U.S.C. § 103 as being unpatentable over the APA in view of *Dabral et al.* (U.S. Patent No. 6,278,312). This rejection is respectfully traversed.

With respect to claims 1-3, 9-12, and 18, the Office Action states:

> With regard to independent claim 1 and as shown in Fig. 2 of the present application, the APA discloses a bus, including a clock driver (item 210), a clock receiver (item 220) coupled to the clock driver by two clock bus lines (items 270 and 272) carrying complementary clock pulses, a plurality of drivers (items 202, 204, and 206) a plurality of receivers (items 221, 214, and 216) each coupled to a respective one of the plurality of drivers by bus lines (items 262, 264, and 266). With regard to dependent claim 9, the APA teaches the bus, further including a plurality of outputs (items 282, 284, and 286) from the data receivers coupled to a deskew/retiming logic component (item 240).
>
> With regard to independent claim 10 and dependent claims 11, 12, and 18, and as shown in Fig. 1 of the present application, the APA discloses a data processing system (item 100), including a plurality of components (*e.g.*, items 102, 108, 104, etc.), and a bus (item 106) coupling at least two of the plurality of components. The APA also discloses the features of claims 10 and 18 as described with respect to claims 1 and 9 above.
>
> The APA does not expressly disclose the bus or the data processing system where the receivers detect signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses, as described in independent claim 1. As shown in Fig. 4B, Dabral discloses a reference voltage (item 433) derived from a combination of complementary clock pulses (SIGNAL and SIGNAL#).
>
> With regard to dependent claims 2 and 11, the APA does not expressly disclose the bus or the data processing system where the reference voltage is derived from a resistive connection between the complementary clock pulses. As shown in Fig. 4B, Dabral discloses a reference voltage (item 433) derived from a resistive connection (items 432 and 434) between the complementary clock pulses (SIGNAL and SIGNAL#).
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> With regard to dependent claims 3 and 12, the APA does not expressly disclose the bus or the data processing system where resistors in

the resistive connection have an approximately equivalent resistance. As described in column 6, lines 9-12, Dabral discloses resistors in the resistive connection that have an approximately equivalent resistance.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the reference voltage and resistor configuration of Dabral with the APA. The suggestion or motivation for doing so would have been to reduce or eliminate driver noise from the data signals (column 1, lines 44-59).

Therefore, it would have been obvious to combine Dabral with the APA to obtain the invention as specified in claims 1-3, 9-12, and 18.

Office Action, dated October 27, 2003. Applicant respectfully disagrees. Claims 1 and 10 are amended to recite a bus apparatus wherein each clock bus line is split terminated such that each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair. The allegedly admitted prior art and *Dabral*, taken alone or in combination, fail to teach or suggest "wherein each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair," as recited in amended claim 1. The applied prior art fails to teach or suggest each and every claim limitation; therefore, claim 1 cannot be rendered obvious by the proposed combination of allegedly admitted prior art and *Dabral*.

Independent claim 10 recites subject matter addressed above and is allowable for the same reasons. Since claims 2, 3, 9, 11, 12, and 18, as well as new claims 19-22 depend from claims 1 and 10, the same distinctions between the allegedly admitted prior art and *Dabral* and the invention recited in claims 1 and 10 apply for these claims. Additionally, claims 2, 3, 9, 11, 12, and 18-22 recite other additional combinations of features not suggested by the reference.

Therefore, the rejection of claims 1-3, 9-12, and 18 under 35 U.S.C. § 103 is overcome.

The Office Action rejects claims 5-8 and 14-17 under 35 U.S.C. § 103 as being unpatentable over the APA in view of *Dabral* as applied to claims 1, 2, 10, and 11 above, and further in view of *Oakeson et al.* (U.S. Patent No. 6,456,123). This rejection is respectfully traversed.

With respect to claims 5-8 and 14-17, the Office Action states:

As described above, the APA in view of Dabral discloses the features of claims 1, 2, 10, and 11. With regard to claims 5-8 and 14-17,

> the APA in view of Dabral does not expressly disclose a first filter capacitor connecting the reference voltage signal to ground, and a second filter capacitor connecting the reference voltage to a supply voltage source. Also, the APA in view of Dabral also does not expressly disclose the bus or the data processing system, where the first and second filter capacitors have an approximately equivalent capacitance, and where the capacitance is within a range of approximately 100 pico-farads and approximately 200 pico-farads.
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> As shown in Fig. 3, Oakeson discloses a first filter capacitor (item C2) connecting the reference voltage signal to ground, and a second filter capacitor (item C1) connecting the reference voltage to a supply voltage source (item 11). In addition, Oakeson discloses the first and second filter capacitors having an approximately equivalent capacitance, (column 5, lines 29-36), and within the range of approximately 100 pico-farads and approximately 200 pico-farads (column 5, lines 38-45).
>
> At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the capacitor configuration of Oakeson with the APA in view of Dabral. The suggestion or motivation for doing so would have been to reduce the susceptibility to inaccuracies caused by parasitics (column 1, lines 8-24).
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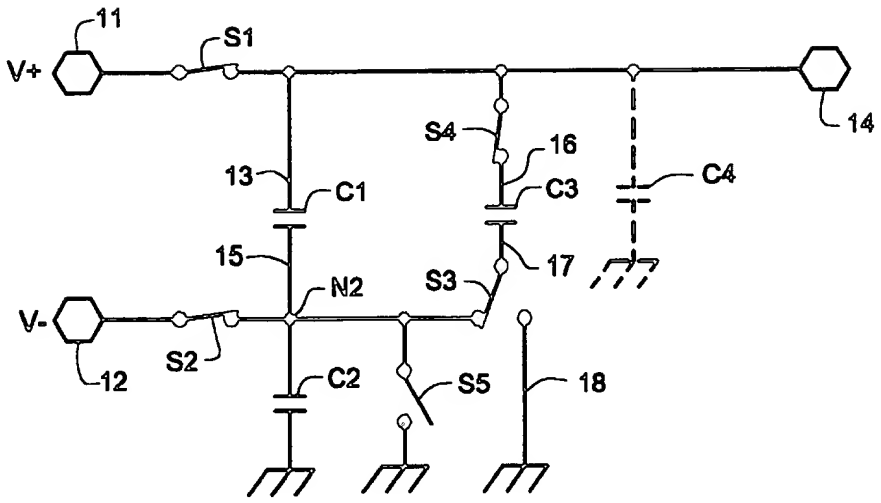
> Therefore, it would have been obvious to combine Oakeson with the APA in view of Dabral to obtain the invention as specified in claims 5-8 and 14-17.

Office Action, dated October 27, 2003. Applicant respectfully disagrees. The allegedly admitted prior art, *Dabral*, and *Oakeson*, taken alone or in combination, fail to teach or suggest "a first filter capacitor connecting said reference voltage signal to ground," as recited in claim 5, and "a second filter capacitor connecting said reference voltage to a supply voltage source," as recited in claim 6.

Oakeson teaches a translation circuit for transferring a differential voltage to a ground referenced voltage. See *Oakeson*, Abstract. That is, the translation circuit receives a signal on two complementary bus lines and outputs a single signal that is relative to ground. The translation circuit includes a sample/hold (S/H) circuit for holding the values of the complementary bus lines that make up the signal. Figure 2 of *Oakeson* is reproduced below:



Capacitor C2 connects a first differential signal lines to ground. Capacitor C1 connects the first differential signal line to a second differential signal line. There is no mention whatsoever of a reference voltage in *Oakeson*, particularly a **reference voltage** being derived from a combination of complementary **clock** pulses. Figure 3 of *Oakeson*, and the description thereof, also fail to show a supply voltage source. Therefore, *Oakeson* does not teach or suggest a first filter capacitor connecting the reference voltage signal to ground and a second filter capacitor connecting the reference voltage to a supply voltage source, as alleged in the Office Action. The allegedly admitted prior art and *Dabral* also fail to teach or suggest these features. Since the applied prior art fails to teach or fairly suggest each and every claim limitation, claims 5 and 6, the proposed combination of allegedly admitted prior art, *Dabral*, and *Oakeson* does not render these claims obvious.

Independent claim 14 recites subject matter addressed above with respect to claim 5 and is allowable for the same reasons. Since claims 6-8 and 15-17 depend from claims 5 and 14, the same distinctions between the allegedly admitted prior art, *Dabral*, and *Oakeson* and the invention recited in claims 5 and 14 apply for these claims. Additionally, claims 6-8 and 15-17 recite other additional combinations of features not suggested by the reference.

Furthermore, as evidenced by the attached Declaration under 37 CFR § 1.131 and the accompanying exhibits, drawings, and records, the present invention was invented prior to the effective date of the *Oakeson* reference. 35 U.S.C. 102(e) reads as follows:

A person shall be entitled to a patent unless -

(e) the invention was described in - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The patent to Oakeson et al. was not filed in the United States before **the invention by the applicant**. *Oakeson* also does not qualify as prior art under any other section of 35 U.S.C. 102. Therefore, the rejection based upon *Oakeson* must be withdrawn.

Therefore, the rejection of claims 5-8 and 14-17 under 35 U.S.C. § 103 is overcome.

IV. Conclusion

It is respectfully urged that the subject application is patentable over the prior art of record and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 26, 2004

Respectfully submitted,

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Attached: Declarations under 37 CFR § 131; Invention Disclosure; record of file creation date